Referring to FIG.1, a block diagram of a circuit 10 illustrating a conventional phase lock loop based spread spectrum clock generator is shown. The circuit 10 generates a signal OUT in response to (i) a reference signal REF and a command signal SSON. The signal REF is presented to an input prescaler 12 and a multiplexer 14. The signal OUT is presented to a feedback prescaler 20 and a multiplexer 22. The signal SSON is presented to (i) the control inputs of the multiplexers 14 and 22 and (ii) the spread spectrum circuitry 26. In response to the command signal SSON, (i) the multiplexer 14 selects between the reference signal REF and an output of the input prescaler 12, (ii) the multiplexer 22 selects between the output signal OUT and an output of the feedback prescaler 20 and (iii) the spread spectrum circuitry modulates the signal out.

A1

Please replace the paragraph beginning at page 4, line 11 with the following paragraph:

Referring to FIG. 2, a timing diagram and an oscilloscope tracing illustrating signals of the circuit 10 are shown. The timing diagram illustrates that a transition 30 in the signal SSON results in an immediate transition at the control inputs of the multiplexers 14 and 22. A portion 40 of the oscilloscope tracing

A2 CONT

illustrates the large transient response of the circuit 10 when spread spectrum modulation is switched on.

A2 cont'd

Please replace the paragraph beginning at page 9, line 16 with the following paragraph:

The circuit 114 generally comprises, in one example, an input prescaler 140, a multiplexer 142, an input divider 144, a phase lock loop (PLL) 146, a feedback prescaler 148, a multiplexer 150, a feedback divider 152, a spread spectrum circuit 154, and a ROM 156. The signal REF is generally presented to an input 158 of the input prescaler 140 and an input 160 of the multiplexer 142. An output 162 of the input prescaler 140 is generally connected to an input 164 of the multiplexer 142. The signal SSON_A is generally presented to a control input 166 of the multiplexer 142. An output 168 of the multiplexer 142 is generally connected to an input 170 of the input divider 144. An output 172 of the input divider 144 is generally connected to an input 174 of the PLL 146. The signal FDBCK is generally presented to an input 176 of the PLL 146. The PLL 146 may be configured to generate the signal CLK.

A3

Please replace the abstract with the following paragraph:

A circuit and method for controlling a spread spectrum transition are presented comprising a first circuit and a second circuit. The first circuit may be configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal. The second circuit may be configured to synchronize the command signal to a feedback signal. The sequence of spread spectrum ROM codes may be generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

A4